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EP-A-0 114 435
EP-A-0 179 693

IEDM TECHNICAL DIGEST, dec.1-4, pages 234-237, 1985, Washington, USA; S.BAMPI et al.:"Modified LDD device structures for VLSI"

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Description

Background of the Invention

Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on}xA$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltge range of two hundred fifty to three hundred volts, $R_{on}xA$ is typically 10—15 Ωmm^2. A discrete vertical D—MOS device in the same voltage range has a figure of merit of $3\Omega mm^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

US—A—4,626,879 shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom expitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediat epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON"-resistance.

US—A—4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

A MOS transistor comprising the feature of the pre-characterizing portion of claim 1 is known from IEDM Technical Digest, Dec. 1—4, 1985, Washington, USA, pages 234—237, S. Bampi et al. "Modified LDD device structures for VLSI". The highest voltages contemplated range up to five volts.

Summary of the Present Invention

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a 300 volt n-channel device with a figure of merit, $R_{on} \times A$, of about $2.0\ \Omega mm^2$.

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0\ \Omega mm^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

In the Drawings

Fig. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

Fig. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

Fig. 3 is a diagrammatic view of the transistors shown in Figs. 1 and 2 forming a complementary pair on the same chip.

Fig. 4 is a diagrammatic view of low voltage, C—MOS implemented devices that can be combined on the same chip with the complementary

pair of high voltage MOS transistors shown in Fig. 3.

Fig. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

Description of the Preferred Embodiment

Looking now at Fig. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p^+ material and a pocket 21 of n^+ material are diffused into the p^- substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material of avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n^+ material is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D—MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/cm^2$ to around $2 \times 10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D—MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D—MOS device (0.7 volts compared to two—four volts for the D—MOS device) and thus, is directly compatible with five volt logic. The D—MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that later will be in the range of 5×10^{16}—$1 \times 10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about 20 Ωmm^2 for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10—15 Ωmm^2, while the best discrete vertical D—MOS devices on the market in a similar voltage range have a figure of merit of 3—4 Ωmm^2.

With reference to Fig. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n^+ type material and a pocket 36 of p^+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from beneath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-

implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extending drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p^+ drain contact pocket 38 and the n-well.

Looking now at Fig. 3, an n-channel transistor 10, similar to that shown in Fig. 1, and a p-channel transistor 30, similar to that shown in Fig. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to Figs. 1 and 2, no further description is considered necessary.

As shown in Fig. 4, low voltage, C—MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in Fig. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p^+ pocket 49 and an n^+ pocket 51 are provided in the p^- substrate beneath the source contact. The n^+ pocket extends to beneath the gate. An n^+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n^+ pocket 58 and a p^+ pocket 59 are provided in the n-well beneath the source contact and a p^+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated in an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complementary transistors are formed on the same chip, the well in which one complementary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

Fig. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n^+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dioxide layer thereabove. Beneath the drain contact is an n^+ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source and an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 Ωmm^2. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Claims

1. A high voltage MOS transistor (10; 30) comprising:

a semiconductor substrate (11; 33) of a first conductivity type having a surface,

a pair of laterally spaced pockets (21, 24; 36, 38)

of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact (14; 31) connected t ne pocket (21; 36),

a drain contact (16; 32) connected to the other pocket (24; 38),

a drain region (26; 37) of the second conductivity type extending laterally from the drain contact pocket (24; 38) to a surface-adjoining position,

a surface-adjoining layer (27; 39) of material of the first conductivity type on top of an intermediate portion of the drain region (26; 37) between the drain contact pocket (24; 38) and the surface-adjoining position,

said substrate (11; 33) being subject to application of a reverse-bias voltage,

an insulting layer (12) on the surface of the substrate (11; 33) and covering at least that portion between the souce contact pocket (21; 36) and the nearest surface-adjoining position of the drain region (26; 37), and

a gate electrode (17, 34) on the insulating layer (12) and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket (21; 36) and the nearest surface-adjoining position of the drain region (26; 37), said gate electrode (17; 34) controlling by field-effect the flow of current thereunder through the channel, characterized in that

said drain region (26; 37) is an extended one extending laterally each way from the drain contact pocket to the surface-adjoining positions, and said surface-ajoining layer (27; 39) extends between the drain contact pocket (24; 38) and the surface-adjoining positions and is physically connected to said substrate (11; 33) so that biasing said substrate (11; 33) means also biasing said surface-adjoining layer (27; 39).

2. The high voltage MOS transistor (10) of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor (30) of an opposite channel conductivity type combined on the same chip and isolated from each other (Fig. 3).

3. The high voltage MOS transistor (10) of claim 1 combined on the same chip with a low voltage CMOS implement device (43).

4. The combination of claim 3 further including a complementary high voltage MOS transistor (30) and a complementary low voltage CMOS implemented device (44) on the same chip and isolated from each other.

5. The high voltage MOS transistor of any of the preceeding claims comprising:

an extended souce region (71) of the second conductivity type extending laterally each way from the source contact pocket (72) to surface-adjoining positions,

a surface-adjoiing layer (73) of material of the first conductivity type on top of an intermediate portion of the extended source region (71) between the surface-adjoining p sitions,

said top layer (73) and said substrate (68) being subject to application of a reverse-bias voltage.

6. Th high-voltage MOS transistor of claim 1 wherein said top layer (27; 39) has a depth of one micrometer or less.

7. The high-voltage MOS transistor of claim 1 wherein said top layer (27; 39) has a doping density higher than $5 \times 10^{16}/cm^3$ so that the mobility starts to degrade.

Patentansprüche

1. MOS-Hochspannungstransistor (10; 30) mit einem Halbleitersubstrat (11; 33) eines ersten Leitfähigkeitstyps, das eine Oberfläche besitzt,

einem Paar von in seitlichem Abstand angeordneten Wannen (21, 24; 36, 38) aus einem Halbleitermateiral eines zweiten Leitfähigkeitstyps innerhalb des Substrats und angrenzend an die Substratoberfläche,

einem mit einer Wanne (21; 36) verbundenen Source-Kontakt (14; 31),

einem mit der anderen Wanne (24; 38) verbundenen Drain-Kontakt,

einer Drain-Zone (26; 37) des zweiten Leitfähigkeitstyps, die sich seitlich von der Drain-Kontaktwanne (24; 38) zu einer an die Oberfläche angrenzenden Position erstreckt,

einer an die Oberfläche anschließenden Zone (27; 39) aus einem Material des ersten Leitfähigkeitstyps auf der Oberseite eines mittleren Teils der Drain-Zone (26; 37) zwischen der Drain-Kontaktwanne (24; 38) und der an die Oberfläche angrezenden Position,

wobei das Substrat (11; 33) an eine Spannung in Sperrichtung angelegt ist,

einen Isolierschicht (12) auf der Oberfläche des Substrats (11; 33), die wenigstens den Teil zwischen der Source-Kontaktwanne (21; 36) und der nächsten, an die Oberfläche angrenzenden Position der Drain-Zone (26; 37) bedeckt, und einer Gate-Elektrode (17; 34) auf der Isolierschicht (12), die elektrisch von der Substratzone unter der Gate-Elektrode isoliert ist, welche einen Kanal seitlich zwischen der Source-Kontaktwanne (21; 36) und der nächsten, an die Oberfläche angrenzenden Position der Drain-Zone (26, 37) bildet, wobei die Gate-Elektrode (17, 34) durch einen Feldeffekt den Stromfluß durch den Kanal unter der Elektrode steuert, dadurch gekennzeichnet,

daß die Drain-Zone (26; 37) größere Ausdehnung ha und sich seitlich nach jeder Richtung von der Drain-Kontaktwanne zu den an die Oberfläche angrenzenden Positionen erstreckt, und daß sich die an die Oberfläche angrenzende Schicht (27; 39) zwischen der Drain-Kontaktwanne (24; 38) und den an die Oberfläche angrenzenden Positionen erstreckt und physikalisch mit dem Substrat (11; 33) verbunden ist, so daß eine Vorspannung des Substrats (11; 33) auch eine Vorspannung der an die Oberfläche angrenzenden Schicht (27; 39) bedeutet.

2. MOS-Hochspannungstransistor (10) nach

Anspruch 1 mit einem Kanal eines Leitfähigkeitstyps in Kombination mit einem komplementären MOS-Hochspannungstransistor (30) mit einem Kanal des entgegengesetzten Leitfähigkeitstyps, die auf dem gleichen Halbleiterplättchen kombiniert und voneinander isoliert sind (Fig. 3).

3. MOS-Hochspannungstransistor (10) nach Anspruch 1 in Kombination mit einem CMOS-Bauteil (43) niedriger Spannung auf dem gleichen Halbleiterplättchen.

4. Kombination nach Anspruch 3 mit ferner einem komplementären MOS-Hochspannungstransistor (30) und einem komplementären CMOS-Bauteil (44) niedriger Spannung, die isoliert voneinander auf dem gleichen Halbleiterplättchen angeordnet sind.

5. MOS-Hochspannungstransistor nach einem der vorhergehenden Ansprüche mit

einer ausgedehnten Source-Zone (71) des zweiten Leitfähigkeitstyps, die sich seitlich nach jeder Richtung von der Source-Kontaktwanne (72) zu an die Oberfläche angrenzenden Positionen erstreckt,

einer an die Oberfläche angrenzenden Schicht (73) aus einem Material des ersten Leitfähigkeitstyps oberhalb eines mittleren teils der ausgedehnten Source-Zone (71) zwischen den an die Oberfläche angrenzenden Positionen, wobei die oberhalb angeordnete Schicht (73) und das Substrat (68) an eine Vorspannung in Sperrichtung angelegt sind.

6. MOS-Hochspannungstransistor nach Anspruch 1, bei dem die oberhalb angeordnete Schicht (27; 39) eine Tiefe von einem Mikrometer oder weniger hat.

7. MOS-Hochspannungstransistor nach Anspruch 1, bei dem die oberhalb angeordnete Schicht (27; 39) eine Dotierdichte größer als $5 \times 10^{16}/cm^3$ besitzt, so daß die Ladungsträgerbeweglichkeit beginnt schlechter zu werden.

Revendications

1. Transistor MOS (10; 30) à tenue en tension élevée, comprenant:

un substrat semiconducteur (11; 33) d'un premier type de conductivité, possédant une surface,

une paire de poches (21, 24; 36, 38) mutuellement espacées latéralement, en matériau semiconducteur d'un second type de conductivité, prévues dans le substrat et contiguës à la surface du substrat,

un contact de source (14; 31) connecté à une poche (21; 36),

un contact de drain (16; 32) connecté à l'autre poche (24; 38),

une région de drain (26; 37) du second type de conductivité, s'étendant latéralement depuis la poche (24; 38) du contact de drain à un point contigu à la surface,

une couche (27; 39) contiguë à la surface, en matériau du premier type de conductivité, disposée par-dessus un partie intermédiaire de la région de drain (26; 37) entre la poche (24; 38) du contact de drain et le point contigu à la surface,

le substrat (11; 33) étant destiné à recevoir une tension de polarisation inverse,

une couche isolante (12) prévue sur la surface du substrat (11; 33) et recouvrant au moins la partie située entre la poche (21; 36) du contact de source et le point le plus proche contigu à la surface de la région de drain (26; 37), et

une électrode de grille (17, 34) disposée sur la couche isolante (12) et isolée électriquement de la région de substrat située sous elle, laquelle forme un canal s'étendant latéralement entre la poche (21; 36) du contact de source et le point le plus proche contigu à la surface de la région de drain (26; 37), l'électrode (17; 34) commandant, par effet de champ, la circulation de courant paracourant le canal sous elle, caractérisé en ce que

la région de drain (26; 37) est une région de drain étendu, s'étendant latéralement vers chaque côté à partir de la poche du contact de drain jusqu'aux points contigus à la surface, et la couche (27; 39) contiguë à la surface s'étend entre la poche (24; 38) du contact de drain et les points contigus à la surface et est physiquement connectée au substrat (11; 33), de sorte que la polarisation de ce substrat (11; 33) produit également la polarisation de la couche (27; 39) contiguë à la surface.

2. Transistor MOS (10) à tenue en tension élevée selon la revendication 1, possédant un type de conductivité de canal, en combinaison avec un transistor MOS (30) complémentaire, à tenue en tension élevée, ayant un type de conductivité de canal opposé, les deux transistors étant combinés sur la même pastille et étant isolés l'une de l'autre (Fig. 3).

3. Transistor MOS (10) à tenue en tension élevée selon la revendication 1, combiné sur la même pastille avec un dispositif (43), constitué par un CMOS, à tenue en tension basse.

4. Combinaison selon la revendication 3, comportant en outre un transistor MOS (30) complémentaire, à tenue en tension élevée, et un dispositif complémentaire (44), constitué par un CMOS et à faible tenue en tension, qui sont prévus sur la même pastille et sont isolés l'une de l'autre.

5. Transistor MOS (10) à tenue en tension élevée selon l'une quelconque des revendications précédentes, comprenant:

une région de source étendue (71) du second type de conductivité, s'étendant latéralement vers chaque côté à partir de la poche (72) du contact de source vers des points contigus à la surface,

une couche (73) contiguë à la surface, en matériau du premier type de conductivité, disposée par-dessus une partie intermédiaire ou centrale de la région de source étendue (71), entre les points contigus à la surface, cette couche de recouvrement (73) et le substrat (68) pouvant recevoir une tension de polarisation inverse.

6. Transistor MOS à tenue en tension élevée selon la revendication 1, dans lequel la couche de recouvrement (27; 39) possède une profondeur d'un micromètre ou moins.

7. Transistor MOS à tenue en tension élevée

selon la revendication 1, dans lequel la couche de recouvrement (27; 39) présente une densité de dopage supérieure à $5 \times 10^{16}/cm^3$, de sorte que la mobilité commence à se dégrader.

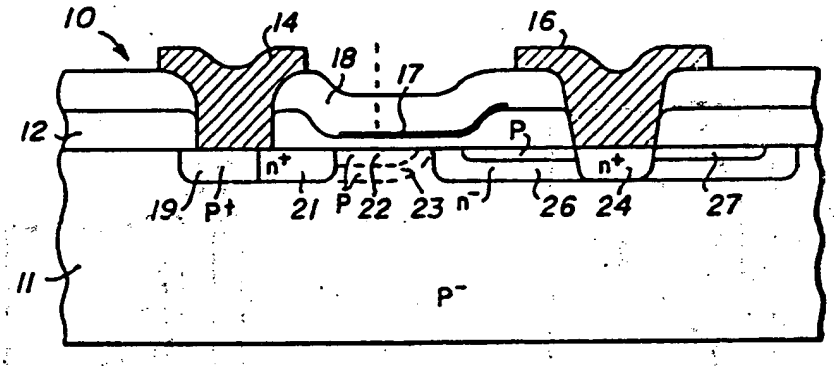

Fig_1

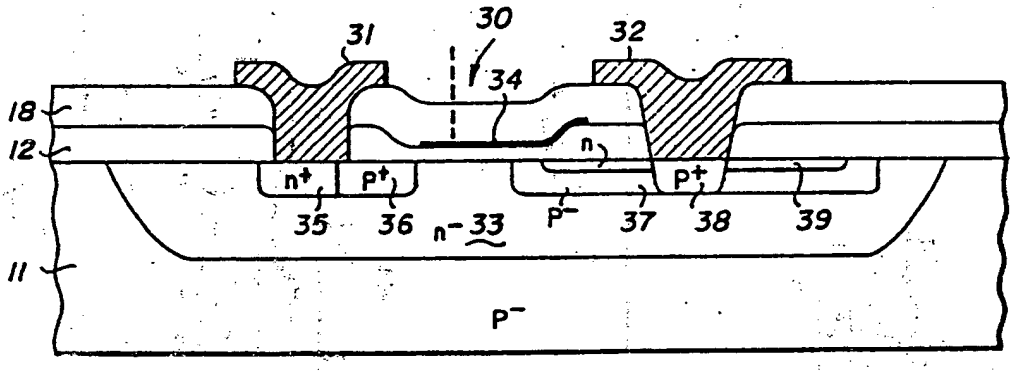

Fig_2

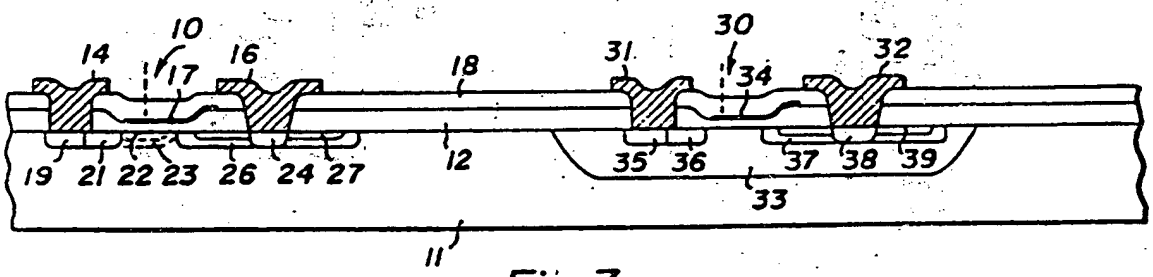

Fig_3

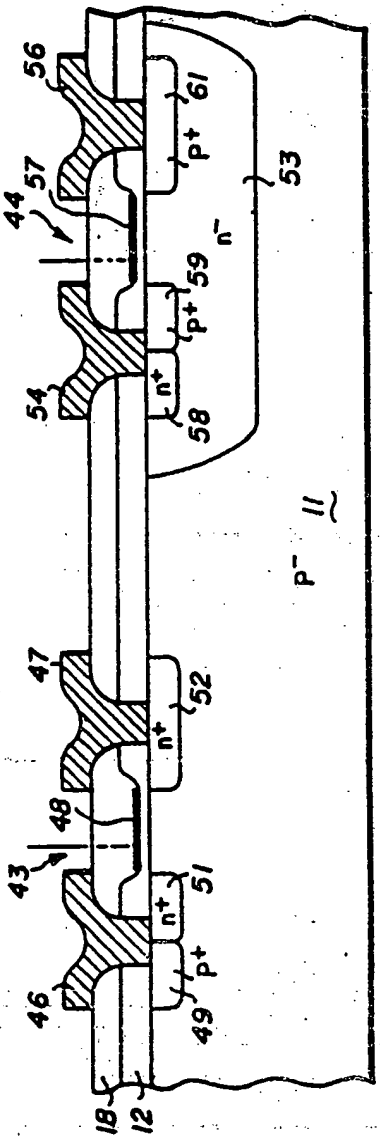
56
57
44
61
p+
53
n⁻
59
p+
54
n+
58
47
52
n+
48
43
51
n+
46
p+
49
18
12
P⁻ 11

Fig-4

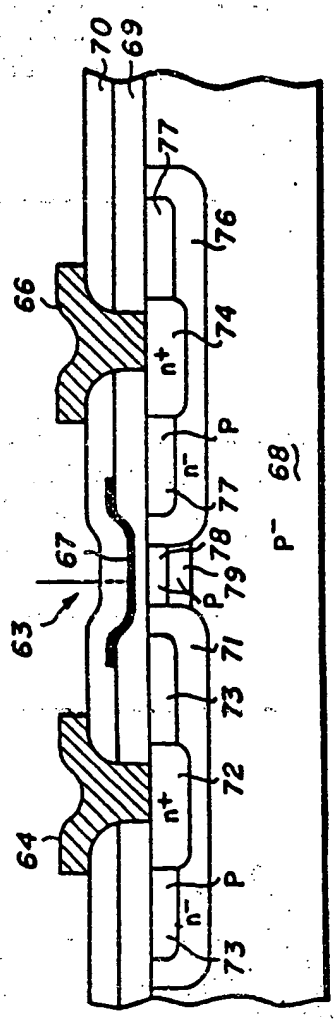
70
69
77
66
76
74
n+
P
n⁻
77
67
78
79
63
P
71
73
72
n+
64
P
n⁻
73
P⁻ 68

Fig-5